ZAPO 捷博科技

W23

WiFi Single-band 1X1

Module Datasheet

Revision History

Version	Date	Description	Draft	Approved
1.0	2017-06-01	First release	Colin Ming	William Tan
1.1	2017-06-22	Modified input voltage range	Colin Ming	William Tan
1.1	2017-06-22	Added 32.768K clock input requesting	Colin Ming	William Tan
1.2	2017-07-14	Modified Pin13、39、40 function	Colin Ming	William Tan

CONTENTS

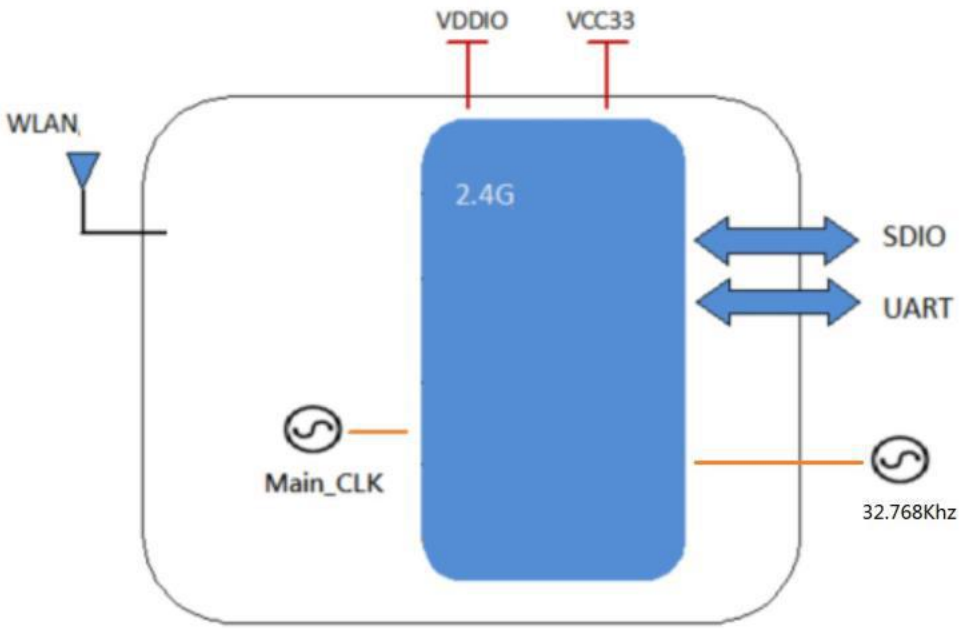
1. Introduction

W23 is a small size and low profile of WiFi module, board size is 12mm*12mm with module thickness of 1.7mm. It can be easily manufactured on SMT process and highly suitable for tablet PC, ultra book, mobile device and consumer products. It providesSDIO interface for WiFi. The WiFi throughput can go up to 150Mbps in theory by using 1x1 802.11b/g/n MIMO technology.

W23 uses highly integrated WiFi single chip based on advanced COMS process. W23 integrates whole WiFi function blocks into a chip, such as SDIO/MPU, MAC, BB, AFE, RFE, PA, EEPROM and LDO/SWR, except fewer passive components remained on PCB.

This compact module is a total solution for Wi-Fi technology. The module is specifically developed for Smart phones and Portable devices.

The block diagram of module is depicted in the figure below.



2. Features

Operate at ISM frequency bands (2.4GHz)
SDIO interface for WiFi
Low power dissipation
High transmitting power
High receiving sensitivity
IEEE standards support: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n.
Enterprise level security which can apply WPA/WPA2 certification for WiFi.
WiFi 1 transmitter and 1 receiver allow data rates supporting up to 150 Mbps downstream and 150 Mbps upstream PHY rates

3. General Specification

3.1 General Specification

Model Name	W23
Product Description	Support WiFi functionality
Dimension	L x W x H: 12 x 12 x1.8 (typical) mm
WiFi Interface	Support SDIO
Operating temperature	-30°C to 70°C
Storage temperature	-40°C to 125°C

3.1.2 Recommended Operating Rating

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	70	deg.C
VCC33	3.3	-	4.8	V
VDDIO	-	1.8V	-	V

4. WiFi RF Specification

4.1 2.4GHz RF Specification

Feature	Description
Operating Frequency	2.400～2.4835GHz
Standards	WiFi: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n, IEEE 802.11d, IEEE 802.11e, IEEE 802.11h, IEEE 802.11i
Modulation	WiFi: 802.11b: CCK(11, 5.5Mbps), QPSK(2Mbps), BPSK(1Mbps), 802.11 g/n: OFDM
PHY Data rates	WiFi: 802.11b: 11,5.5,2,1 Mbps 802.11g: 54,48,36,24,18,12,9,6 Mbps 802.11n: up to 150Mbps
Transmit Output Power	WiFi: 802.11b@11Mbps 19±1.5dBm 802.11g@54Mbps 17±1.5dBm 802.11n@65Mbps 16±1.5dBm (MCS 7_HT20) 15±1.5dBm (MCS 7_HT40)
EVM	802.11b /1Mbps : EVM≦-10dB 802.11b /11Mbps : EVM≦-10dB 802.11g /6Mbps : EVM≦-5dB 802.11g /54Mbps : EVM≦-25dB 802.11n /6.5Mbps : EVM≦-5dB 802.11n /65Mbps : EVM≦-28dB 802.11n /13.5Mbps : EVM≦-5dB 802.11n /135Mbps : EVM≦-28dB
Receiver Sensitivity (WiFi)	802.11b@10% PER 1Mbps≦-98dBm 2Mbps≦ -94dBm 5.5Mbps≦ -93dBm 11Mbps≦-90dBm Max input level≥-8
	802.11g@10% PER 6Mbps≦-94dBm

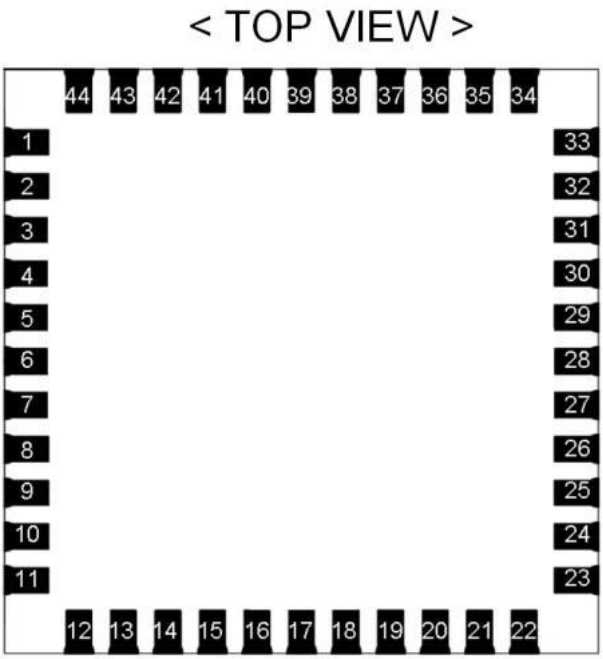
	9Mbps≦ -92dBm 12Mbps≦ -91dBm 18Mbps≦ -89dBm 24Mbps≦ -86dBm 36Mbps≦ -82dBm 48Mbps≦-78dBm 54Mbps≦-77dBm Max input level≥-20
	802.11n@10% PER HT20_MCS 0≦-93dBm HT40_MCS 0≦-90 HT20_MCS 1≦ -90dBm HT40_MCS 1≦-87 HT20_MCS 2≦-88dBm HT40_MCS 2≦-85 HT20_MCS 3≦-85dBm HT40_MCS 3≦-82 HT20_MCS 4≦-82dBm HT40_MCS 4≦-79 HT20_MCS 5≦-78dBm HT40_MCS 5≦-75 HT20_MCS 6≦-76dBm HT40_MCS 6≦-73 HT20_MCS 7≦-75dBm HT40_MCS 7≦-71 Max input level≥-20
Operating Channel	WiFi 2.4GHz: 11: (Ch. 1-11) – United States 13: (Ch. 1-13) – Europe 14: (Ch. 1-14) – Japan
Media Access Control	WiFi: CSMA/CA with ACK
Antenna	External Antenna
Network Architecture	Ad-hoc mode (Peer-to-Peer) Infrastructure mode Software AP WiFi Direct
Security	WPA, WPA-PSK, WPA2, WPA2-PSK, WEP 64bit & 128bit, IEEE 802.11x, IEEE 802.11i
OS Supported	Android /Linux/XP/WIN7
Host Interface	SDIO
Operating Voltage	3.3-4.8V Vdc I/O supply voltage
Dimension	Typical 12*12*1.8 mm

5. Power Consumption

Power Consumption (Typical by using SWR)	TX Mode: (Throughput mode) 230mA (MCS7/BW40/16dBm) RX Mode: (Throughput mode) 66mA (MCS7/BW40/-60dBm) Associated Idle power saving with DTIM=3 0.38mA Deep Sleep: 0.04mA

6. Pin Assignments

6.1 Pin Outline



6.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	NC	—	Floating (Don't connected to ground)
5	NC	—	Floating (Don't connected to ground)
6	Host wake device	I	Host Wake up WiFi, rising edge trigger
7	GPIO3	I/O	Floating (Don't connected to ground)
8	NC	—	Floating (Don't connected to ground)
9	VCC	P	Main power voltage source input 3.3V-4.8V
10	NC	—	Floating (Don't connected to ground)
11	NC	—	Floating (Don't connected to ground)
12	PMU_POWRON	I	Enable pin for WLAN device ON: pull high ; OFF: pull low
13	GPIO1	I/O	SDIO data interrupt
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line

17	SDIO_DATA_CLK	I	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	NC	—	Floating (Don't connected to ground)
22	VDDIO	P	I/O Voltage supply input 1.8V
23	NC	—	Floating (Don't connected to ground)
24	RTC_CLK	I	Exteral 32.768Khz clock input for Power saving
25	NC	—	Floating (Don't connected to ground)
26	NC	—	Floating (Don't connected to ground)
27	NC	—	Floating (Don't connected to ground)
28	NC	—	Floating (Don't connected to ground)
29	NC	—	Floating (Don't connected to ground)
30	NC	—	Floating (Don't connected to ground)
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	GPIO2	I/O	Floating (Don't connected to ground)
35	NC	—	Floating (Don't connected to ground)
36	GND	—	Ground connections
37	NC	—	Floating (Don't connected to ground)
38	NC	—	Floating (Don't connected to ground)
39	WL_RST	I	WiFi reset pin, internal pull high. Low: reset enable, High: reset disable
40	Dev_Wake_Host	O	WiFi wake up host, rising edge trigger for host, high level trigger for MCU.
41	NC	—	Floating (Don't connected to ground)
42	NC	—	Floating (Don't connected to ground)
43	NC	—	Floating (Don't connected to ground)
44	NC	—	Floating (Don't connected to ground)

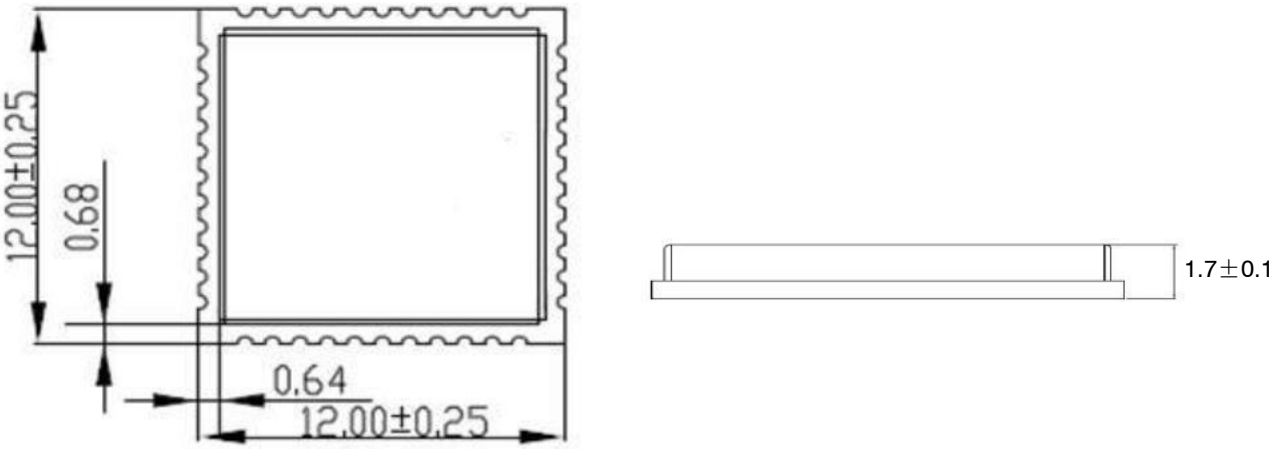
7. Dimensions

7.1 Physical Dimensions

(Unit: mm)

< TOP VIEW >

< Side View >



Marking Description

< TOP VIEW >

7.2 Module Physical Dimensions

(Unit: mm)

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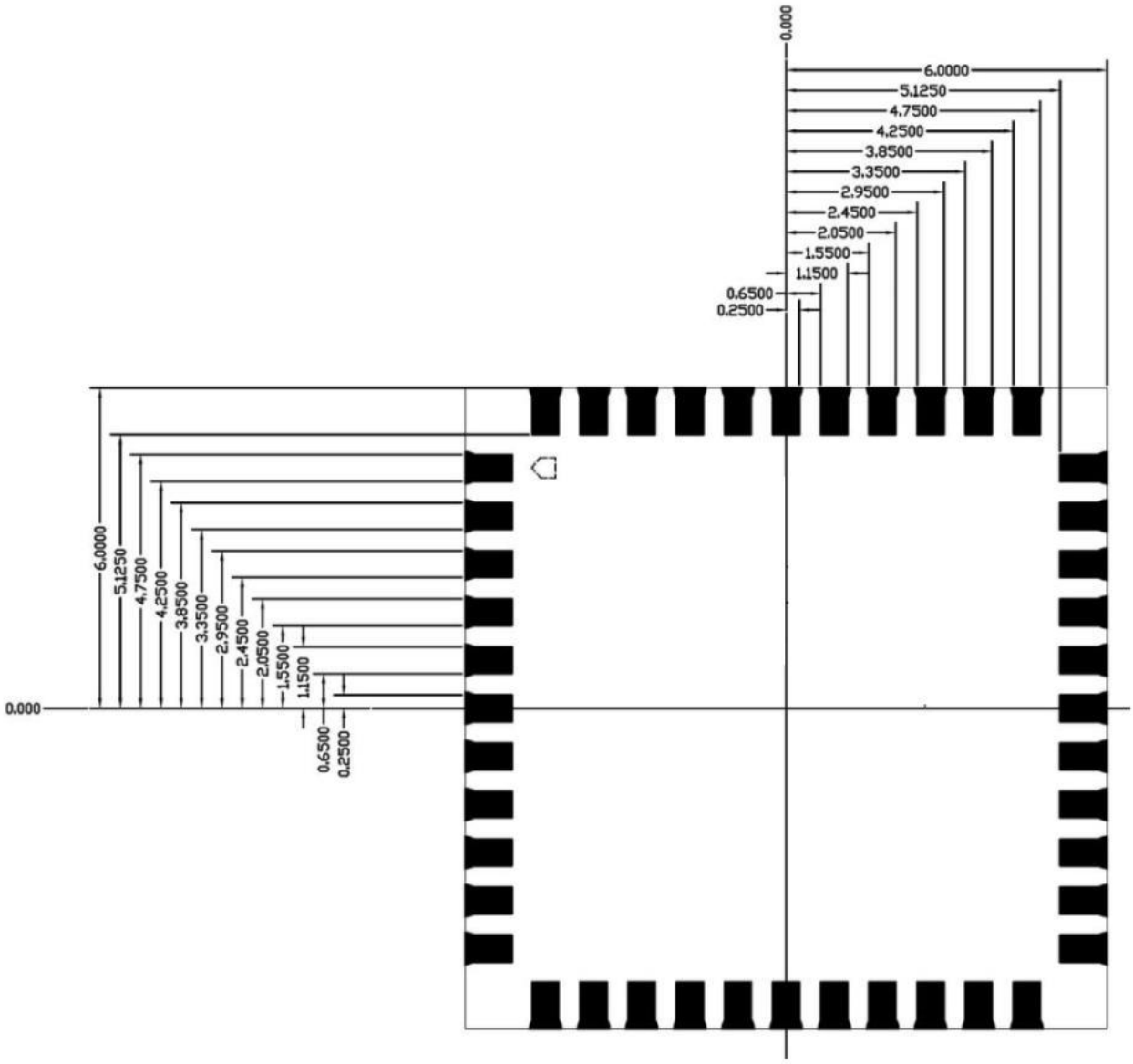
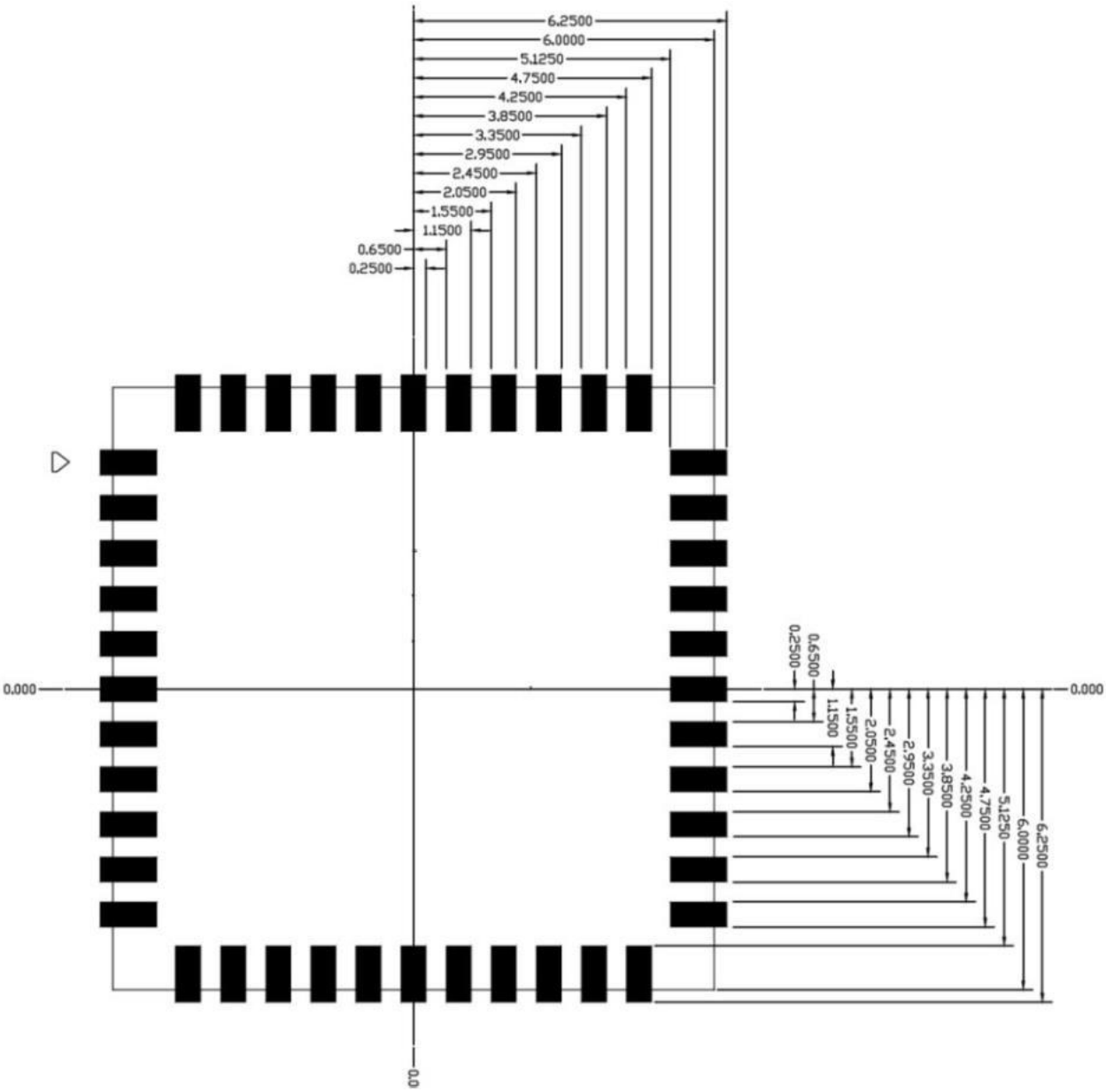


7.3 Layout Recommendation

(Unit: mm)

< TOP VIEW >



8. Host Interface Timing Diagram

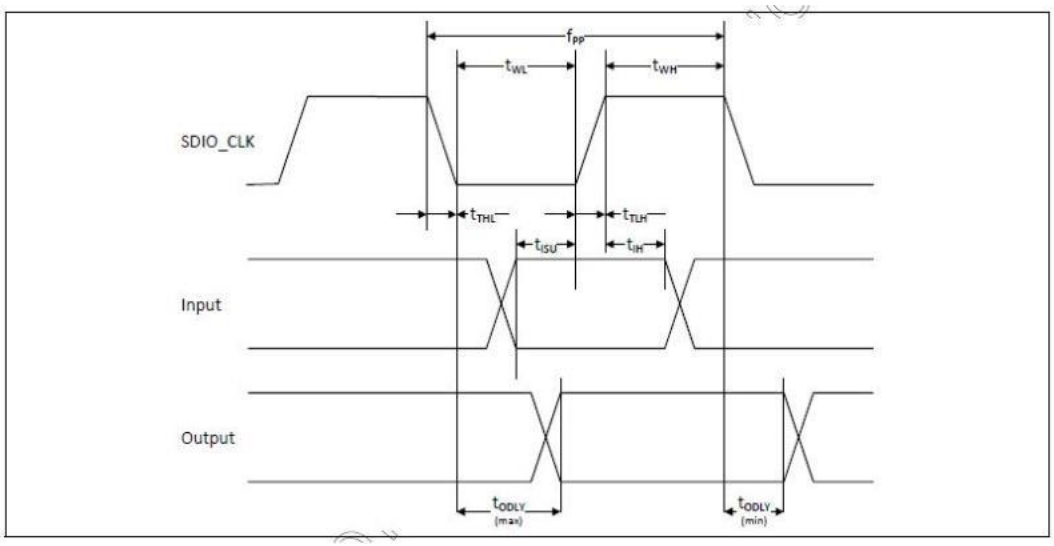
8.1 SDIO Pin Description

The module supports SDIO version 2.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps),SDR104(208MHz) and DDR50(50MHz, dual rates) in addition to the 1.8V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

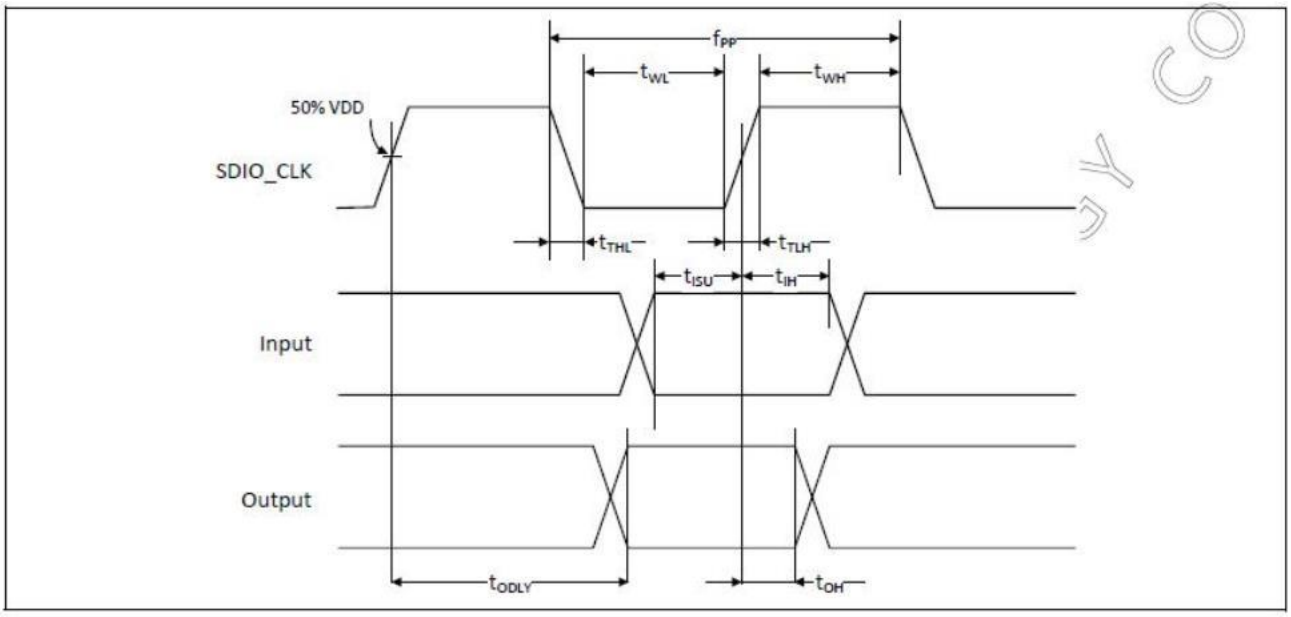
8.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

8.3 SDIO High Speed Mode Timing Diagram

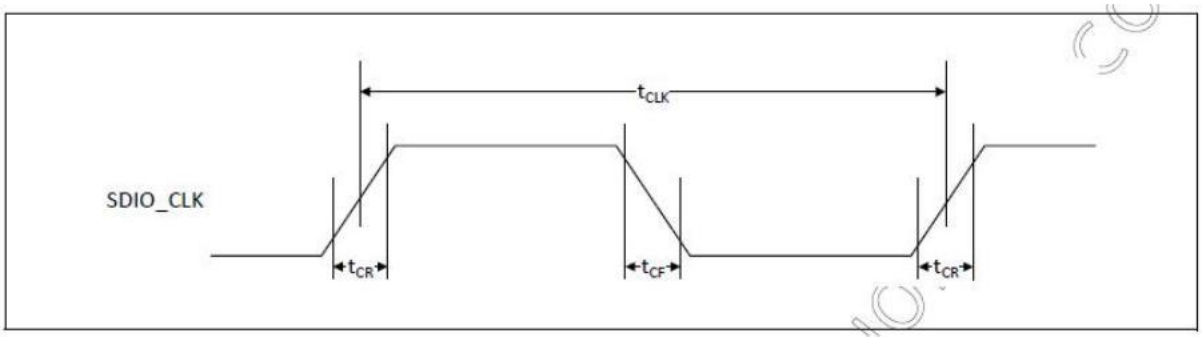


Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

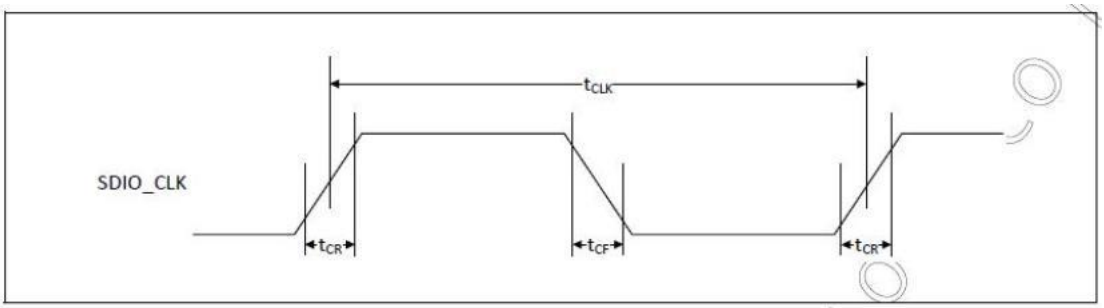
a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

8.4 SDIO Bus Timing Specifications in SDR Modes

Clock timing(SDR Modes)

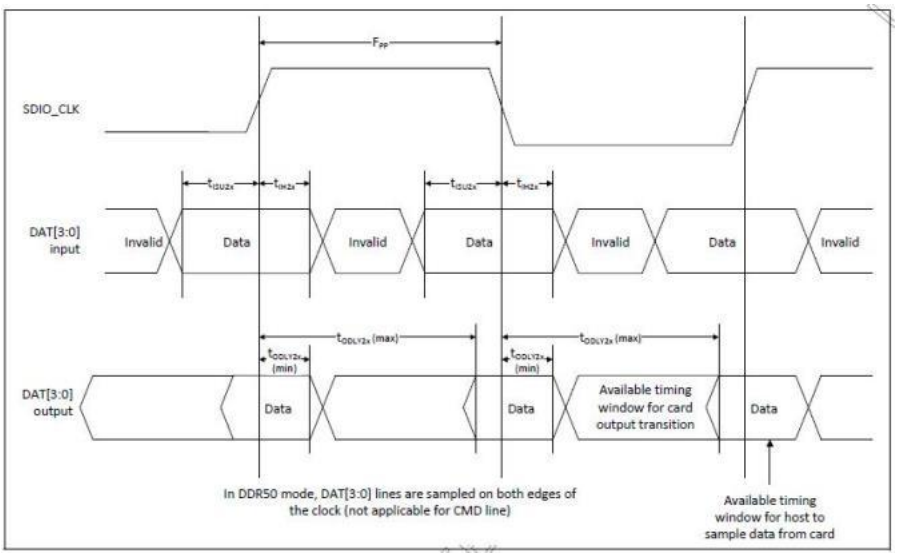


8.5 SDIO Bus Timing Specifications in DDR50 Mode



Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
–	t_{CLK}	20	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45	55	%	–

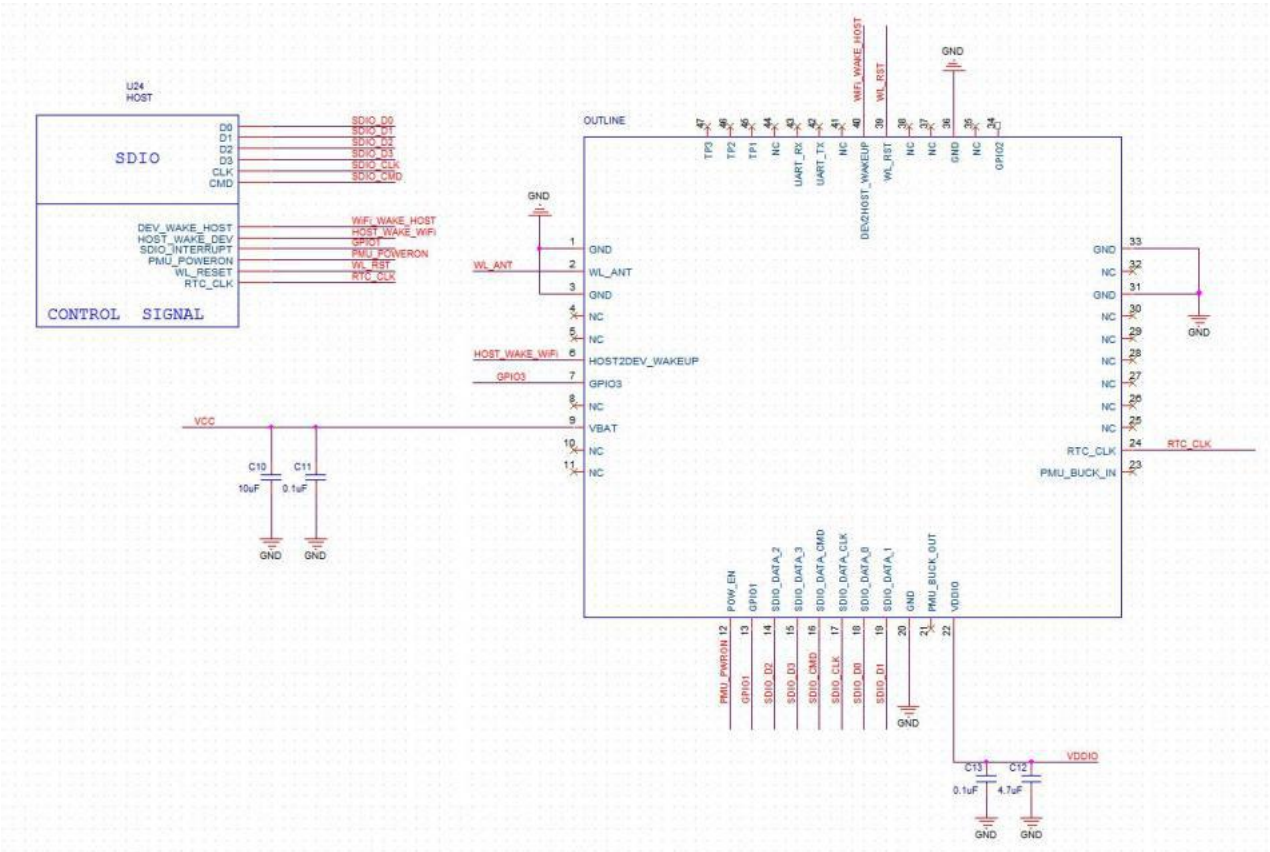
Data Timing



Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.85[a]	ns	C_{CARD} < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15pF (1 Card)

a. SDIO 3.0 specification value is 7.0 ns.

9.Reference Design

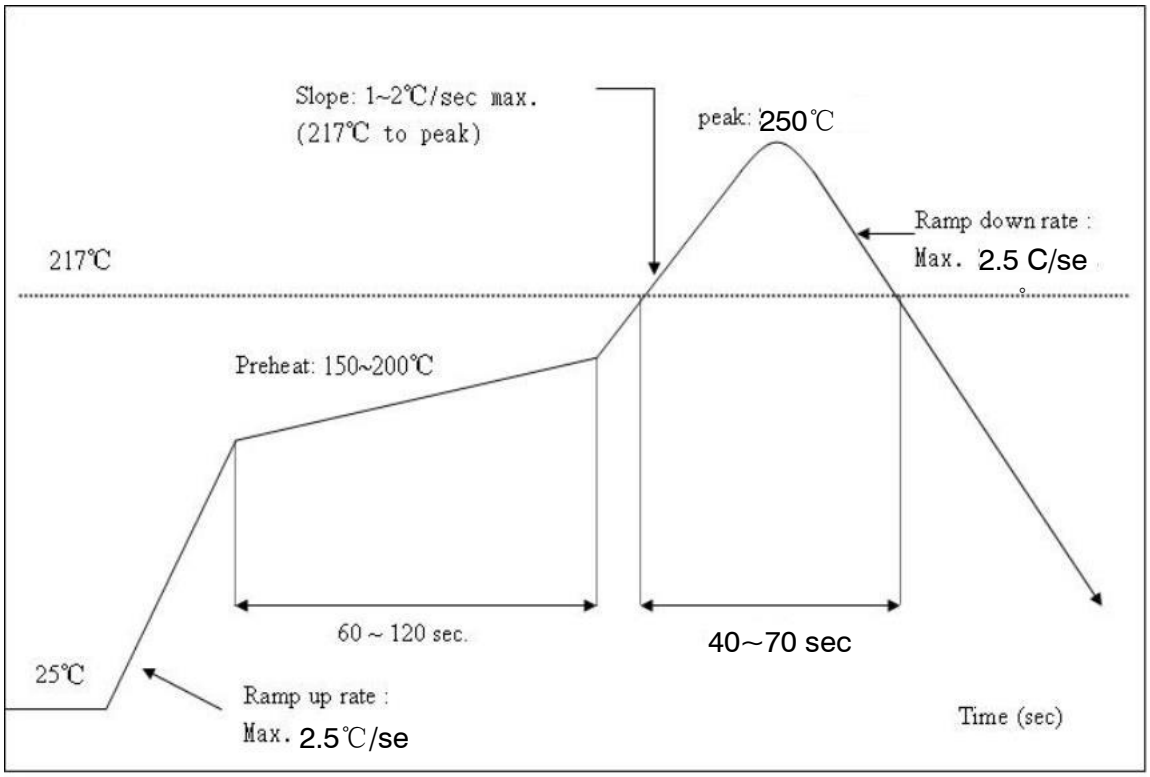


10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : 2 times



11. Packing Information

Tape and Reel Package

Using self-adhesive tape

Size of black tape: 24mm*32.6m the cover tape: 21.3mmm*32.6m

Color of plastic disc: blue

A roll of 2000pcs

NY bag size:460mm*385mm size：350*350*35mm