Product Specification

QCA9377-3 Dual-Band 1x1 802.11ac and Bluetooth v4.1 Combo Module

Project Name	QCA9377-3 WiFi+BT Combo
_	LGA Module
Part No.	W9377
Model Name.	-

Content

3
4
4 4
5
5 5
8
11
. 11
FICATIONS 11

0. Revision History

⊔ate	Document revision	Author	Change Description
2015/3/31	0.1	Andy. Tu	Initial release(draft)
2015/4/10	0.2	Andy. Tu	Update LGA pin-out and Mechanical Drawing
2015/07/10	0.3	Rachel.wu	Update RF characteristics
2015/07/27	0.4	Rachel.wu	 Change LGA Pin#6 signal from NC to Host_wakeup_BT in section2.3 Update the reflow profile in section7.6

1. Introduction

Project Name: QCA9377-3 WLAN+BT Combo LGA Module

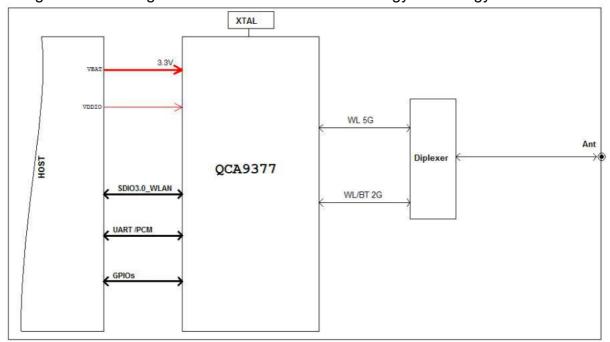
Project Number: W9377

This documentation describes the engineering requirements specification of QCA9377-3

LGA module. It is a confidential document.

1.1 Scope

This module design is based on the Qualcomm Atheros QCA9377-3 HW v1.1 chipset. The QCA9377-3 is a single-chip wireless local area network (WLAN) and Bluetooth (BT) combo solution to support 1x1 with IEEE802.11a/b/g/n/ac WLAN standards and BT4.1+HS enabling seamless integration of WLAN/BT and Low Energy technology.



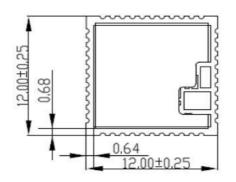
1.2 Function

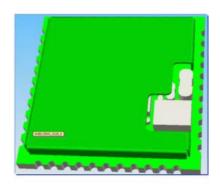
- WLAN dual-band 1x1 IEEE802.11a/b/g/n/ac and Bluetooth V4.1+HS
- Support WLAN 20MHz/40MHz at 2.4GHz and 20/40/80 MHz at 5GHz
- Support BT4.1+HS, BLE and be backwards compatible with BT1.x,2.x+EDR.
- Support BT for class 1 and class 2 power level transmissions without requiring an external PA.
- Support low-power SDIO3.0 interface for WLAN and UART/PCM interface for BT
- Support Multi-user MiMO
- Support WiFi/BT coexistence
- Both WLAN and BT power management utilize advanced power saving techniques:
 - √ clock gating on idle or inactive blocks;
 - ✓ voltage scaling on specific blocks in certain states;
 - ✓ fast start and settling circuits to reduce Tx;
 - ✓ active duty cycles, processor frequency scaling,
 - ✓ and other techniques to optimize power consumption across all operating states. Including additional features such as: Low-Density Parity Check(LDPC)
- One-chip one-time programmable(OTP) memory
- GP/HF compliance

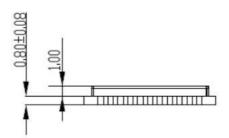
2. Mechanical Specification

2.1 Mechanical Drawing

Typical module dimension (W x L): 12mm x12mm. The Z-height is 1.85mm (typical) and 1.98mm (max)

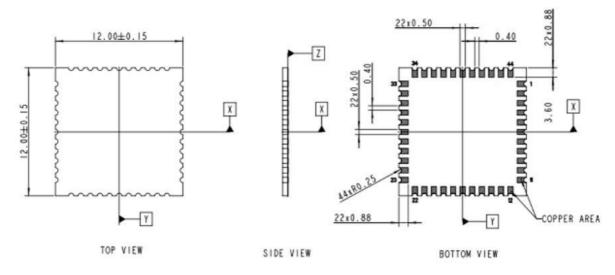






Unit: mm

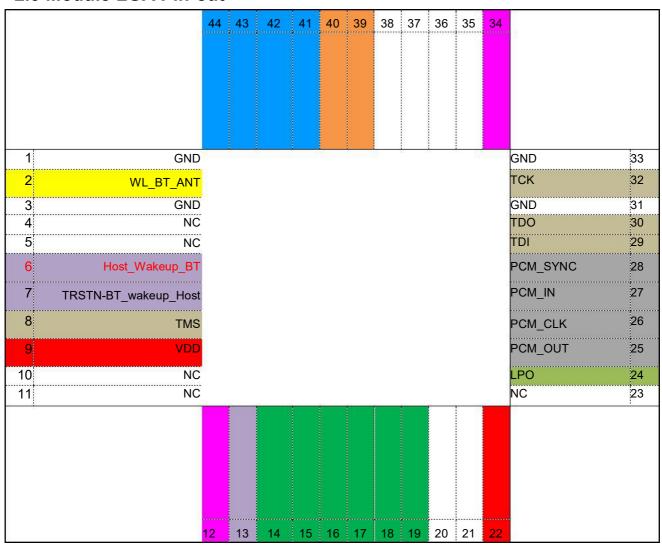
2.2 Recommended LGA Land Pattern



Unit: mm

Suggest use "solder-mask on pad" design for main-board LGA pad

2.3 Module LGA Pin-out



Signal Group	Pin No.	Signal	I/O	Description	Voltage	Connecting
	9	VDD	ı	DC power supply +3.3V input	3.3V	Yes
Power	22	VDDIO	I	External power source input for VIO domain. Default use 1.8V for SDIO3.0 mode	1.8V or 3.3V	Yes
Ground	1,3,20,31, 33,36	GND		Return current path	0V	Yes
ANT	2	WL_BT_ANT	I/O	Wi-Fi/BT RF signal	-	Yes
Control	12	WL_EN	I	GPIO pin to on/off the Wi-Fi function by software. Active high. Reserve pull high 100K resistor and shunt 100pF capacitor to GND on platform.	VDDIO	Yes
Control	34	BT_EN	I	GPIO pin to on/off the BT function by software. Active high. Reserve pull high 100K resistor and shunt 100pF capacitor to GND on platform.	VDDIO	Yes

(1)	24	LPO	I	External low-power 32.768KHz clock input.	VDDIO	Yes
	13	WL_wakeup_Host	0	WLAN device wakeup platform	VDDIO	Yes
	6	Host_wakeup_BT	I	Host/platform wakeup BT device	VDDIO	Yes
	14	SDIO_DATA2	I/O	SDIO data2 exchange,	VDDIO	Yes
	15	SDIO_DATA3	I/O	SDIO data3 exchange	VDDIO	Yes
	16	SDIO_CMD	I/O	SDIO Command Interface	VDDIO	Yes
SDIO	17	SDIO_CLK	ı	SDIO 3.0 Clock	VDDIO	Yes
	18	SDIO_DATA0	I/O	SDIO data0 exchange	VDDIO	Yes
	19	SDIO_DATA1	I/O	SDIO data1exchange	VDDIO	Yes
	41	UART RTS	0	UART Ready To Send, connected to CTS on the platform.	VDDIO	Yes
	42	UART_TXD	0	UART Transmit Data, connected to RXD on the platform.	VDDIO	Yes
	43	UART_RXD	I	UART Receive Data, connected to TXD on the platform.	VDDIO	Yes
UART/	44	UART CTS	I	UART Clear To Send, connected to RTS on the platform.	VDDIO	Yes
PCM	25	PCM_OUT	0	PCM synchronous data output, connected to PCM_IN on the platform.	VDDIO	Yes
	26	PCM_CLK	I/O	PCM Clock	VDDIO	Yes
	28	PCM_SYNC	I/O	PCM synchronous data SYNC	VDDIO	Yes
	27	PCM_IN	I	PCM synchronous data input, connected to PCM_OUT on the platform.	VDDIO	Yes
UART_De	39	Debug_UART_TXD	0	TXD for Wi-Fi Uart_debug only, connected to RXD of the platform.	VDDIO	Option
bug	40	Debug_UART_RXD	I	RXD for Wi-Fi Uart_debug only, connected to TXD of the platform.	VDDIO	Option
	7	TRSTN &BT_wakeup_Host	I/O	1.BT wakeup platform 2.Reserve for EJTAG	VDDIO	Yes
JTAG_De	8	TMS	I/O	Reserve for EJTAG	VDDIO	Option
bug	29	TDI	I	Reserve for EJTAG	VDDIO	Option
	30	TDO	0	Reserve for EJTAG	VDDIO	Option
8	32	TCK	I/O	Reserve for EJTAG	VDDIO	Option
Others	4,5,10,11, 21,23,35, 37,38	NC		No Connect		No

3. Electrical Specification

3.1 Absolute Maximum Ratings

These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended can adversely affect long-term reliability of the device.

Symbol	Condition	Min.	Тур.	Max	Unit
VDD	Respect to GND	-0.3	3.3	3.63	V
Max Ripple on Supplied Voltage	3.3V			330	mVpp
Storage Temperature		-40	25	+85	$^{\circ}$
ESD(HBM)				2000	V

3.2 Recommended Operating Condition

Symbol	Condition	Min.	Тур.	Max	Unit
VDD	Respect to GND	3.135	3.3	3.465	V
VDDIO	Respect to GND	1.71	1.8 or 3.3	3.46	V
Operating Temperature		-10	+25	+70	°C

Function operation is not guaranteed outside this limit, and operation outside this limit for extended periods can adversely affect long-term reliability of the device.

3.3 Digital Logic Characteristics

Table 1 General DC Electrical Characteristics (for 1.8V VIO Operation)

Symbol	Parameter	Condition	Min.	Max	Unit	Notes
+3.3V	Power supply		3.3-5%	3.3+5%	V	
VIH	High-level input voltage		0.7-VIO	VIO+0.3	V	
VIL	Low-level input voltage		-0.3	0.3-VIO	V	
IIL	Input low leakage current		-5	5	uA	
VOH	High-level output voltage		VIO-0.4	VIO	V	
VOL	Low-level output voltage		0	0.4	V	
ЮН	High-level output voltage		3	-	mA	
IOL	Low-level output current		-	-11	mA	

3.4 RF Characteristics

All typical performance specification are based-on operation at room temperature (+25 $^{\circ}$ C) using default parameter setting and nominal supply voltages at RF connector port.

Note: The target power table maybe updated later based-on final DVT report and official regulatory testing.

.

3	Standard	IEEE802	.11a/	b/g/ı	n/ac									Œ.
	Data Rate		/g: 54 ode: ode:	I, 48 MCS MCS	s, 36, 24, S0~MCS S0~MCS	18, 15,u 15,u	ıp to	72.2M 150MI	Ibps bps					
	Bandwidth	20MHz,4 20MHz, 4					Hz							
	Modulation Techniques	802.11b: 802.11a/g 802.11n: 802.11ac	g: 64 64Q	QAN AM,	И,16QAM 16QAM,	1, QF QPS	PSK SK, I	BPSK		3PSk	<			
	Frequency Range	2.4GHz~ 5.15GHz												
	Media Access Control	CSMA/C	A wit	h AC	CK									
Wi-Fi		OFDM 2G 5G		1L, 19 6 ~ 18 15	2, 5L 24	5S 19 36 17 14			11L 19 48 17 13			115 19 54 17 12	3	
		Nss=1 HT20 2G 5G	MC 18 15	S0	MCS1 18 15	_2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		4	MCS 17 13	5	MC 17 13		MCS7 16.5
	Transmit Output Power (Power tolerance 2G: +/-1.5dB and	Nss=1 HT40 2G 5G	MC 17	S0	MCS1 17 14	_2		ICS3_4 7		MCS 16 13	5	MC 16 13	S6	MCS7 16
	5G:+/-2dB) Note ₁	Nss=1 VHT20 2G 15	MC - 15	S0	MCS1_ - 15	2	MC - 14	S3_4	MC - 13	CS5	MC:	S6	MCS7 - 11	MCS8 - 11
		Nss=1 VHT40	MC 0		MCS1_ 2	MC 3_4		MCS 5	M 6	ICS	MC 7	S	MCS 8	MCS9
		5G	14		14	14		13	1:	3	11		10	9
		Nss=1 VHT80	MC	S0	MCS1	MC 3_4		MCS 5	M 6	ICS	MC 7	S	MCS 8	MCS 9
3		5G	13		13	13		12	12	2	10		9	8

PS:		
	Minimum Receiver Sensitivity	2.4GHz: 11b 1Mbps: -97dBm(typical)@PER<=8% 11b 11Mbps: -90dBm(typical) @PER<=8% 11g 6Mbps: -92dBm(typical)@PER<=10% 11g 54Mbps: -76dBm(typical)@PER<=10% 11n HT20 MCS0: -92dBm(typical)@PER<=10% 11n HT20 MCS7: -73dBm(typical)@PER<=10% 11n HT40 MCS0: -89dBm(typical)@PER<=10% 11n HT40 MCS7: -71dBm(typical)@PER<=10% 11n HT40 MCS7: -71dBm(typical)@PER<=10% 5GHz: 11a 6Mbps: -89dBm(typical) @PER<=10% 11a 54Mbps: -73dBm(typical) @PER<=10% 11n HT20 MCS0: -89dBm (typical)@PER<=10% 11n HT20 MCS0: -89dBm(typical)@PER<=10% 11n HT40 MCS0: -86dBm(typical)@PER<=10% 11n HT40 MCS7: -67dBm(typical)@PER<=10% 11n HT40 MCS7: -67dBm(typical)@PER<=10% 11n HT40 MCS9: -86dBm(typical)@PER<=10% 11n HT40 MCS9: -67dBm(typical)@PER<=10% 11ac VHT40 MCS9 Nss=1: -63dBm(typical)@PER<=10% 11ac VHT40 MCS9 Nss=1: -60dBm(typical)@PER<=10%
	Radio Modulation	FHSS
	Operating Frequency	2.402GHz ~ 2.4835GHz
	Channel Numbers	79 channels with 1MHz BW
	BDR Transmitter Output	
	Power	Typical: +10dBm (class1,it can be changed by BT firmware)
	BDR Power Control	2dB≤Power Control Step≤8dB
	BDR Initial Carrier Freq. Tolerance	≤ ± 75 kHz
	BDR Carrier Frequency Drift	Drift Rate/50us <±20kHz DH1: +/- 25kHz,DH3: +/- 40kHz,DH5: +/- 40kHz
	BDR Modulation Characteristics	140kHz ≤ Δf1avg ≤175kHz Δf2max ≥115kHz Δf2avg/Δf1avg ≥0.8
	BDR Maximum Receiver Signal	-20dBm@ BER <= 0.1% at 1Mbps
	BDR Multi-slot Sensitivity	Typical -90dBm @ BER <= 0.1% at 1Mbps
	BDR Single Sensitivity	Typical -90dBm @BER <= 0.1% at 1Mbps
	EDR Relative Power	P[GFSK]-4dB <p[dpsk]< p[gfsk]+1db<="" td=""></p[dpsk]<>
вт	EDR Stability and Mod Accuracy	-75 kHz <ωi < 75 kHz -10kHz<ω0 <10kHz RMS DEVM<=0.13 for all 8DPSK @3Mbps Peak DEVM<=0.25 for all 8DPSK @3Mbps 99% DEVM<=0.2 for 99% 8DPSK @3Mbps
	BDR Frequency Range	FL>2.4GHz,FH<2.4835GHz
	EDR Sensitivity	Typical -88dBm@BER <= 0.01% at 2Mbps Typical -85dBm@BER <= 0.01% at 3Mbps
	BDR TX Output Spectrum -20dB Bandwidth	≤1MHz
	LE Output Power	≥ -6dBm(Typical)
	LE Modulation Characteristics	225kHz ≤ Δf1avg ≤275kHz; Δf2max ≥185kHz for at least 99.9% test packets; Δf2avg/Δf1avg ≥0.8
	LE Carrier frequency offset and drift	Carrier frequency offset: ±150kHz Carrier Drift: ≤50kHz Drift rate: ≤20kHz/50us
01	LE Receiver Sensitivity	Typical -90dBm@PER <= 30.8%,GFSK,1Mbps

3.5 Operating System Support

Support the Linux & Android operating system on normal driver.

4. Regulatory Certification

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

5. Quality

This combo module shall pass the standard reliability testing.

The product quality must be followed-up by Foxconn factory quality control system.

6. Environmental Requirements and Specifications

6.1 Temperature

6.1.1 Operating Temperature Conditions

The product shall be capable of continuous reliable operation when operating in ambient temperature of -10 $^{\circ}$ C to +70 $^{\circ}$ C.

6.1.2 Non-Operating Temperature Conditions

Neither subassemblies shall be damaged nor shall the operational performance be degraded when restored to the operating temperature when exposed to storage temperature in the range of -40 $^{\circ}$ C to +85 $^{\circ}$ C.

6.2 PCB Bending

The PCB bending spec shall be keep planeness under 0.1mm for both Foxconn and end assembly customer.

6.3 Handling environment

6.3.1. ESD

The product ESD immunity is HBM(Human Body Model) +2000(V) max . Please handle it under ESD protection environment.

This device is ESD sensitive device, it must be protected at all times from ESD, industry-standard ESD precautions should be used at all times.

6.3.2. Terminals

The product is mounted with motherboard through Land Grid Array. In order to prevent poor soldering, please do not touch LGA portion by hand.

6.3.3. Falling

It will cause damage on the mounted components when the product is falling or receiving drop shock. It may cause the product mal-function.

7.4 Storage Condition

7.4.1 Moisture barrier bag before opened

Moisture barrier bag must be stored under 30 degree C, humidity under 85% RH. The calculated shelf life for the dry packed product shall be a 12 months from the bag seal date.

7.4.2. Moisture barrier bag open

Humidity indicator cards must be blue, <30%.

7.5 Baking Condition

Products require baking before mounting if

1. Humidity indicator cards reads >30%

2. Temp <30 degree C, humidity < 70% RH, over 96 hours

Baking condition: 125 degree C, 12 hours

Baking times: 1 time

7.6 Soldering and reflow condition

1) Heating method

Conventional Convection or IR/convection

2) Temperature measurement

Thermocouple d=0.1mm ~ 0.2mm CA (K) or CC (T) at soldering portion or equivalent method.

3) Solder paste composition

Sn/3.0Ag/0.5Cu

- 4) Allowable reflow soldering times: 2 times based on the below reflow soldering profile Recommend only one time reflow soldering for better reliability performance.
- 5) Temperature profile

Reflow profile condition typically used by QCA is given as below

QCA typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temperature range	Lead-free (high-temperature) condition limits		
Preheat	Initial ramp	< 150°C	3°C/sec max		
Soak	Dry out and flux activation	150 to 190°C	75 to 120 sec		
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec		
Reflow	Time above liquidus	220 to 245°C ¹	50 to 70 sec		
Cool down	Cool rate - ramp-to-ambient	< 220°C	6°C/sec max		

^{1.} During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing

